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Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	
Filing Date	
First Named Inventor	Andrew Horch
Art Unit	
Examiner Name	
Attorney Docket Number	C018-D-1

Sheet 1 of 2

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
PF		US- 3,943,549	3-9-1976	Jaecklin et al.	
		US- 4,165,517	8-21-1979	Temple et al.	
		US- 4,281,336	7-28-1981	Sommer et al.	
		US- 4,323,793	4-6-1982	Schutten et al.	
		US- 4,646,121	2-24-1987	Ogura	
		US- 4,829,357	5-9-1989	Kasahara	
		US- 4,864,168	9-5-1989	Kasahara et al.	
		US- 4,982,258	1-1-1991	Baliga	
		US- 5,412,228	5-2-1995	Baliga	
		US- 5,463,344	10-31-1995	Temple	
		US- 5,606,186	02-1997	Noda, Minoru	
		US- 4,825,272	04-1989	Lehmann, Erhard	
		US- 6,104,045	8-15-2000	Forbes et al.	
		US- 6,225,165	5-1-2001	Noble, et al.	
		US- 6,229,161	5-8-2001	Nemati et al.	
		US-			
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FOREIGN PATENT DOCUMENTS						
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11/1/05

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		First Named Inventor	Andrew Horch		
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		Examiner Name			
Sheet	2	of	2	Attorney Docket Number	C018-D-1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
DF		K. DeMeyer, S. Kubicek and H. van Meer, Raised Source/Drains with Disposable Spacers for sub 100 nm CMOS Technologies, Extended Abstracts of International Workshop on Junction Technology 2001.	
DF		Mark Rodder and D. Yeakley, Raised Source/Drain MOSFET with Dual Sidewall Spacers, IEEE Electron Device Letters, Vol. 12, No. 3, March 1991	
DF		Yang-Kyu Choi, Daewon Ha, Tsu-Jae King and Chenming Hu, Nanoscale Ultrathin PMOSFETs with Raised Selective Germanium Source/Drain, IEEE Electron Device Letters, Vol. 22, No. 9, September 2001.	
DF		N. Lindert, Y. K. Choi, L. Chang, E. Anderson, W. C. Lee, T. J. King, J. Bokor, and C. Hu, Quasi-Planar FinFETs with Selectively Grown Germanium Raised Source/Drain, 2001 IEEE International SOI Conference, 10/2001	
DF		T. Ohguro, H. Naruse, H. Sugaya, S. Nakamura, E. Morifuji, H. Kimijima, T. Yoshitomi, T. Morimoto, H.S. Momose, Y. Katsumata, and H. Iwai, High Performance RF Characteristics of Raised Gate/Source/Drain CMOS with Co Salicide, 1998 Symposium on VLSI Technology Digest of Technical Papers	
DF		Hsiang-Jen Huang, Kun-Ming Chen, Tiao-Yuan Huang, Tien-Sheng Chao, Guo-Wei Huang, Chao-Hsin Chien, and Chun-Yen Chang, Improved Low Temperature Characteristics of P-Channel MOSFETs with Si _{1-x} Gex Raised Source and Drain, IEEE Transactions on Electron Devices, Vol. 48, No. 8, August 2001	
DF		Nemati, Farid and Plummer, James, D., A Novel High Density, Low Voltage SRAM Cell with a Vertical NDR Device, VLSI Technology Technical Digest, 6/1998	
DF		Nemati, Farid and Plummer, James, D., A Novel Thyristor-based SRAM Cell (T-RAM) for High-Speed, Low-Voltage, Giga-scale Memories, International Electron Device Meeting Technical Digest, 1999	
DF		Gribnikov, Z.S., Korobov, V.A., and Mitin, V.V., The Tunnel Diod as a Thyristor Emitter, Solid-State Electronics, Vol. 42, No. 9, 1998, pp. 1761-1763	

Examiner Signature	<i>De An</i>	Date Considered	4/11/05
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